### General Description

The MAX4102/MAX4103 op amps combine high-speed performance and ultra-low differential gain and phase while drawing only 5mA of supply current. The MAX4102 is compensated for unity-gain stability, while the MAX4103 is compensated for a closed-loop gain (AVCL) of 2V/V or greater.

The MAX4102/MAX4103 deliver a 250MHz -3dB bandwidth (MAX4102) or a 180MHz -3dB bandwidth (MAX4103). Differential gain and phase are an ultra-low 0.002%/0.002° (MAX4102) and 0.008%/0.003° (MAX4103), making these amplifiers ideal for composite video applications.

These high-speed op amps have a wide output voltage swing of  $\pm 3.4V$  (R<sub>L</sub> = 100 $\Omega$ ) and 80mA current-drive capability.

### Features

- 250MHz -3dB Bandwidth (MAX4102) 180MHz -3dB Bandwidth (MAX4103)
- Unity-Gain Stable (MAX4102)
- ♦ 350V/µs Slew Rate
- Lowest Differential Gain/Phase (R<sub>L</sub> = 150Ω) MAX4102: 0.002%/0.002° MAX4103: 0.008%/0.003°
- Low Distortion (SFDR 5MHz): -78dBc
- 100dB Open-Loop Gain

TOP VIEW

- High Output Drive: 80mA
- Low Power: 5mA Supply Current



#### Applications

Broadcast and High-Definition TV Systems

Pulse/RF Amplifier

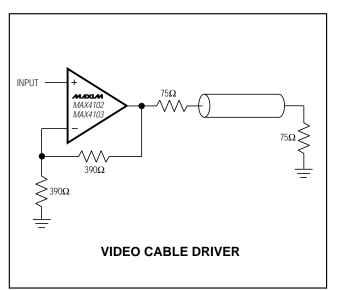
ADC/DAC Amplifier

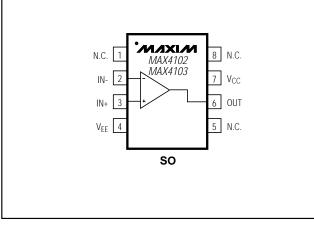
### **Ordering Information**

Pin Configuration

PART	TEMP. RANGE	PIN-PACKAGE
MAX4102ESA	-40°C to +85°C	8 SO
MAX4103ESA	-40°C to +85°C	8 SO

### Typical Application Circuit





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#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V <sub>CC</sub> to V <sub>EE</sub> )12V	
Voltage on Any Pin to Ground or Any Other PinV <sub>CC</sub> to V <sub>EE</sub>	
Short-Circuit Duration (VOUT to GND)Continuous	
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
SO (derate 5.88mW/°C above +70°C)471mW	

Operating Temperature Range	
MAX4102ESA/MAX4103ESA	40°C to +85°C
Storage Temperature Range	65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5V, V<sub>EE</sub> = -5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
DC SPECIFICATIONS	1							
Input Offset Voltage	Vos	Vout = 0V			0.5	8	mV	
Input Offset Voltage Drift	TCVOS	Vout = 0V			5		µV/°C	
Input Bias Current	Ι <sub>Β</sub>	$V_{OUT} = 0V, V_{IN} = -V_{OS}$			3	9	μA	
Input Offset Current	los	$V_{OUT} = 0V, V_{IN} = -V_{OS}$			0.04	0.5	μA	
Common-Mode Input Resistance	RINCM	Either input			5		MΩ	
Common-Mode Input Capacitance	CINCM	Either input			1		рF	
Input Voltage Noise		f = 100kHz	MAX4102		7			
Input voltage Noise	en		MAX4103		5		- nV/√Hz	
Integrated Voltage Noise		f = 1MHz to 100MHz	MAX4102		88		μV <sub>RMS</sub>	
			MAX4103		63			
Input Current Noise		f = 100kHz MAX4102 MAX4103	MAX4102		1.0			
	in			1.0		pA/√Hz		
Integrated Current Noise		f = 1MHz to 100MHz	MAX4102		12.5		nA <sub>RMS</sub>	
Integrated Current Noise			MAX4103		12.5		MARMS	
Common-Mode Input Voltage	Vcm			-2.5		2.5	V	
Common-Mode Rejection	CMR	$V_{CM} = \pm 2.5 V$		75	100		dB	
Power-Supply Rejection	PSR	$V_{S} = \pm 4.5 V \text{ to } \pm 5.5 V$		70	100		dB	
	A	$V_{OUT} = \pm 2.0V$ , $V_{CM} = 0V$	RL = ∞	66	96		dB	
Open-Loop Voltage Gain	$A_{VOL} = \pm 2.0V,$		$R_L = 100\Omega$	70	100		UD	
Quiescent Supply Current	I <sub>SY</sub>	$V_{IN} = 0V$			4.6	6	mA	
Output Voltage Swing	but Voltage Swing $V_{OUT} = \frac{R_L = \infty}{R_L = 100\Omega}$	RL = ∞		±3.3	±3.7		V	
Culput voltage swing		$R_L = 100\Omega$		±3.1	±3.4		v	
Output Current		$R_L = 30\Omega$ , $T_A = 0^{\circ}C$ to $+85^{\circ}C$		65	80		mA	
Short-Circuit Output Current	ISC	Short to ground or either supp	ly voltage		90		mA	

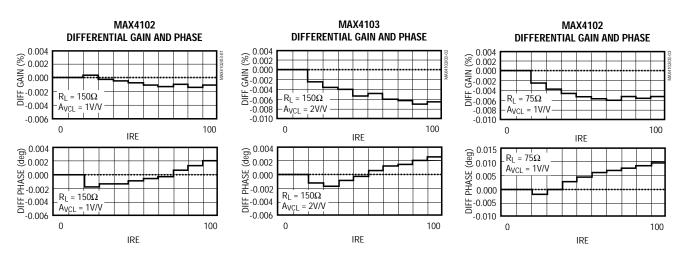
#### **AC ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 5V, V_{EE} = -5V, R_L = 100\Omega, A_{VCL} = +1 (MAX4102), A_{VCL} = +2 (MAX4103), T_A = +25^{\circ}C, unless otherwise noted.)$ 

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS	
AC SPECIFICATIONS	1	L			1			1	
-3dB Bandwidth	BW	V <sub>OUT</sub> ≤ 0.1V <sub>RMS</sub> MAX4102 MAX4103		MAX4102		250		- MHz	
	DVV				180				
0.1dB Bandwidth		MAX4102		130		- MHz			
		MAX4103		80					
Slew Rate	SR	$-2V \le V_{OUT} \le 2V$			350		V/µs		
Cottling Time	+			to 0.1%		18		- ns	
Settling Time	ts	$-1V \le V_{OUT} \le 1V$	V <sub>OUT</sub> ≤ 1V			30			
Rise/Fall Times	to to	10% to 90%, -2V ≤ V <sub>OUT</sub> ≤ 2V			13		ns		
RISE/Fall TIMES	t <sub>R</sub> , t <sub>F</sub>	10% to 90%, -50mV $\leq$ V <sub>OUT</sub> $\leq$ 50mV			1.5				
Differential Gain	DG	f = 3.58MHz,	MAX4102			0.002		%	
Direrential Gain	DG	$R_L = 150\Omega$	MAX4103			0.008		- %	
Differential Phase	DP	f = 3.58MHz,	MAX4102	MAX4102 MAX4103		0.002		dograda	
Differential Phase	DP	$R_L = 150\Omega$	MAX4103			0.003		degrees	
Input Capacitance	CIN		I			2		pF	
Output Resistance	Davia	f 10MU	MAX4102	MAX4102		0.7		Ω	
	Rout	f = 10MHz MAX4103				0.7			
Crawleye Free Durantic D	SFDR	f <sub>C</sub> = 5MHz, MAX4102 V <sub>OUT</sub> = 2V <sub>p-p</sub> MAX4103				-78		dBc	
Spurious-Free Dynamic Range						-76			

### \_Typical Operating Characteristics

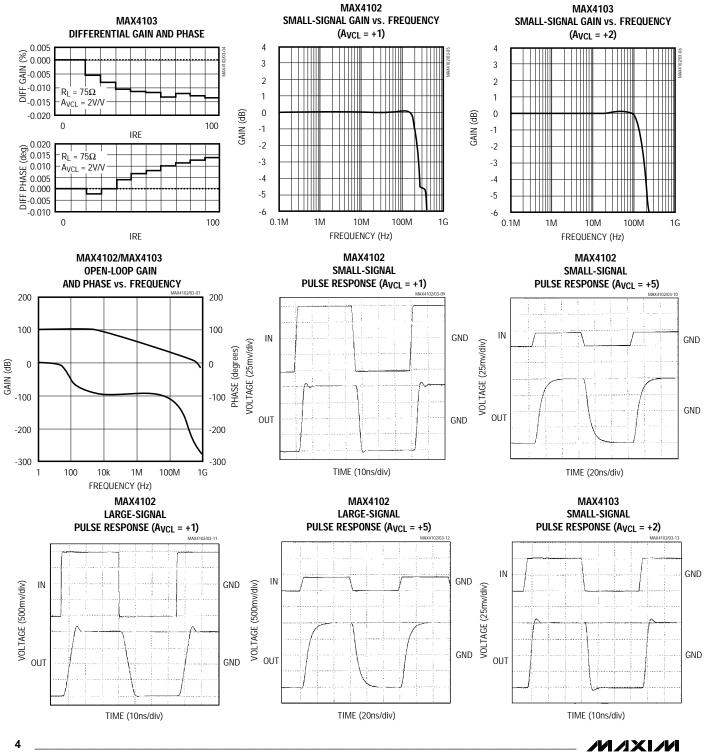
 $(V_{CC} = 5V, V_{EE} = -5V, R_L = 100\Omega, T_A = +25^{\circ}C, unless otherwise noted.)$ 



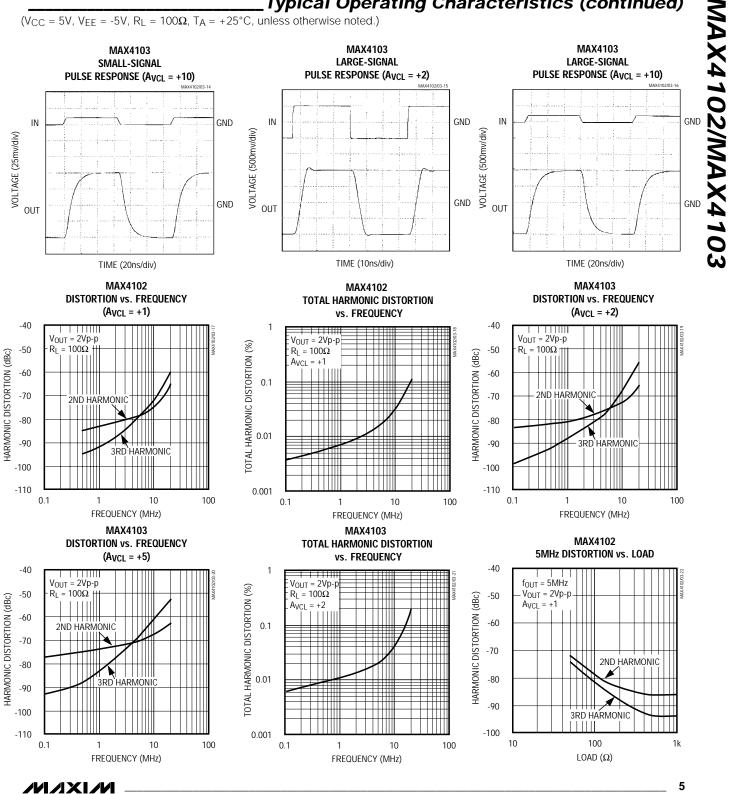
MAX4102/MAX4103

#### Typical Operating Characteristics (continued)

 $(V_{CC} = 5V, V_{EE} = -5V, R_L = 100\Omega, T_A = +25^{\circ}C, unless otherwise noted.)$ 



MAX4102/MAX4103



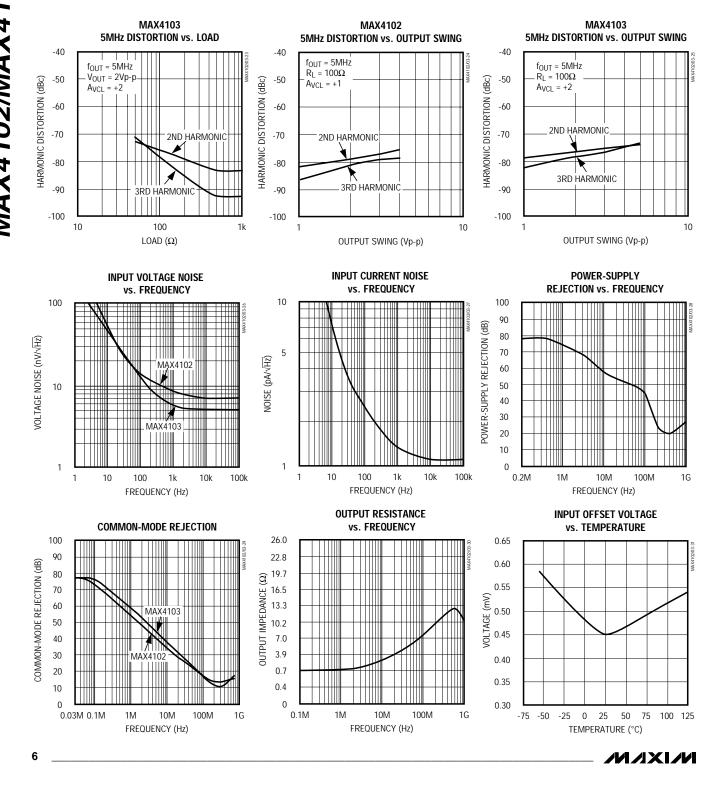
Typical Operating Characteristics (continued)

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#### **Typical Operating Characteristics (continued)**

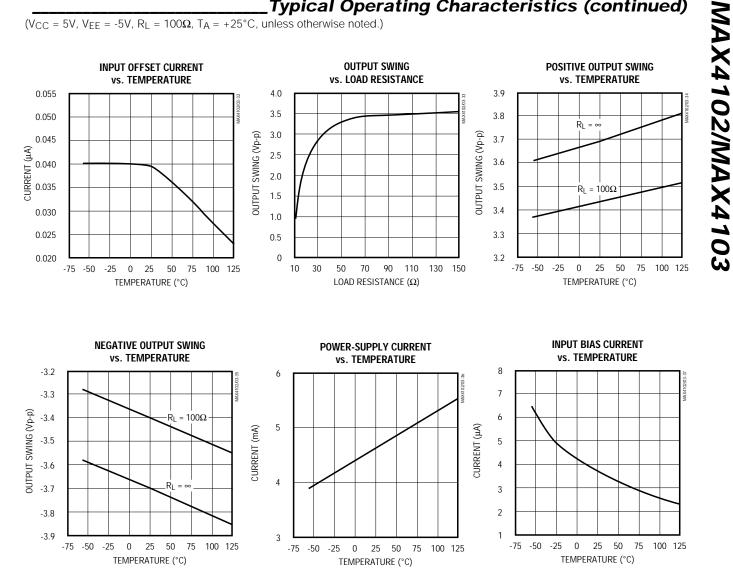
 $(V_{CC} = 5V, V_{EE} = -5V, R_L = 100\Omega, T_A = +25^{\circ}C, unless otherwise noted.)$ 

MAX4102/MAX4103



### Typical Operating Characteristics (continued)

 $(V_{CC} = 5V, V_{EE} = -5V, R_L = 100\Omega, T_A = +25^{\circ}C, unless otherwise noted.)$ 



PIN	NAME	FUNCTION
1	N.C.	Not internally connected
2	IN-	Inverting Input
3	IN+	Noninverting Input
4	V <sub>EE</sub>	Negative Power Supply. Connect to -5V
5	N.C.	Not internally connected
6	OUT	Amplifier Output
7	V <sub>CC</sub>	Positive Power Supply. Connect to +5V
8	N.C.	Not internally connected

### Pin Description

- Do not use wire-wrap boards, because they are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, and give better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

On Maxim's evaluation kit, the ground plane has been removed from areas where keeping the trace capacitance to a minimum is more important than maintaining ground continuity. For example, the ground plane has been removed from beneath the IC to minimize pin capacitance.

The bypass capacitors should include a  $0.1\mu$ F at each supply pin and the ground plane, located as close to the package as possible. Then place a  $10\mu$ F to  $15\mu$ F low-ESR tantalum at the point of entry (to the PC board) of the power-supply pins. The power-supply trace should lead directly from the tantalum capacitor to the V<sub>CC</sub> and V<sub>EE</sub> pins to maintain the low differential gain and phase of these devices.

#### **Setting Gain**

The MAX4102/MAX4103 are voltage-feedback op amps that can be configured as an inverting or noninverting gain block, as shown in Figures 1a and 1b. The gain is determined by the ratio of two resistors and does not affect amplifier frequency compensation.

In the unity-gain configuration (Figure 1c), maximum bandwidth and stability are achieved with the MAX4102 when a small feedback resistor is included. This resistor suppresses the negative effects of parasitic inductance and capacitance. A value of  $24\Omega$  provides the best combination of wide bandwidth, low peaking, and fast settling time. In addition, this resistor reduces the errors from input bias currents.

#### **Choosing Resistor Values**

The values of feedback and input resistors used in the inverting or noninverting gain configurations are not critical (as is the case with current-feedback amplifiers), but should be kept small and noninductive.

### Detailed Description

The MAX4102/MAX4103 low-power, high-speed op amps feature ultra-low differential gain and phase, and are optimized for the highest quality video applications. Differential gain and phase errors are 0.002%/0.002° for the MAX4102 and 0.008%/0.003° for the MAX4103. The MAX4102 also features a -3dB bandwidth of over 250MHz and 0.1dB gain-flatness of 130MHz. The MAX4103 features a -3dB bandwidth of 180MHz and a 0.1dB bandwidth of 80MHz.

The MAX4102 is unity-gain stable, and the MAX4103 is optimized for closed-loop gains of 2V/V (6dB) and higher. Both devices drive back-terminated  $50\Omega$  or  $75\Omega$  cables to  $\pm 3.1V$  (min) and deliver an output current of 80mA.

Available in a small 8-pin SO package, the MAX4102/ MAX4103 are ideal for high-definition TV systems (in RGB, broadcast, or consumer video applications) that benefit from low power consumption and superior differential gain and phase characteristics.

#### Applications Information Grounding, Bypassing, and PC Board Layout

In order to achieve the full bandwidth, Microstrip and Stripline techniques are recommended in most cases. To ensure your PC board does not degrade the amp's performance, it's wise to design the board for a frequency greater than 1GHz. Even with very short runs, it's good practice to use this technique at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:



The input capacitance of the MAX4102/MAX4103 is approximately 2pF. In either the inverting or noninverting configuration, the bandwidth limit caused by the package capacitance and resistor time constant is  $f_{3dB} = 1 / (2\Pi \text{ RC})$ , where R is the parallel combination of the input and feedback resistors (RF and RG in Figure 2) and C is the package and board capacitance at the inverting input. Rs1 and Rs2 represent the input termination resistors. Table 1 shows the typical bandwidth and resistor values for several gain configurations.

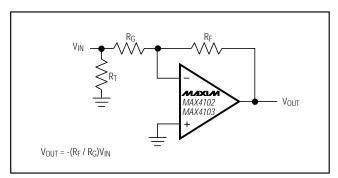


Figure 1a. Inverting Gain Configuration

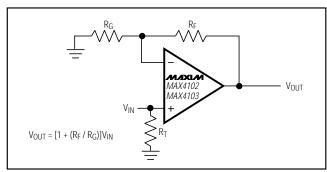


Figure 1b. Noninverting Gain Configuration

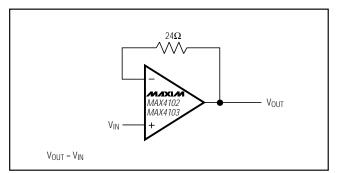


Figure 1c. MAX4102 Unity-Gain Buffer Configuration

## Table 1. Resistor and Bandwidth Valuesfor Various Gain Configurations

DEVICE	GAIN (V/V)	Rg (Ω)	RF (Ω)	<b>Rτ</b> (Ω)	BAND- WIDTH (MHz)
MAX4102	1	∞	24	50	250
MAX4102	2	200	200	50	100
MAX4103	2	200	200	50	180
MAX4103	5	50	200	50	40
MAX4103	10	30	270	50	20
MAX4103	-1	200	200	56	180
MAX4103	-2	75	150	150	140
MAX4103	-5	50	250	∞	75
MAX4103	-10	50	500	∞	35

**Note:** Refer to Figure 1a for inverting gain configurations and Figure 1b for noninverting gain configurations.  $R_T$  is calculated for 50 $\Omega$  systems.

#### **Resistor Types**

Surface-mount resistors are the best choice for highfrequency circuits. They are of similar material to the metal-film resistors, but are deposited using a thick-film process in a flat, linear manner so that inductance is minimized. Their small size and lack of leads also minimize parasitic inductance and capacitance, thereby yielding more predictable performance.

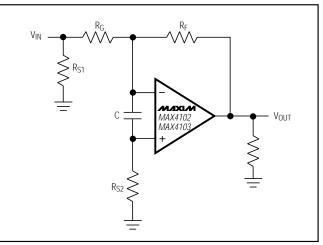


Figure 2. Effect of Feedback Resistor Values and Parasitic Capacitance on Bandwidth

#### **Driving Capacitive Loads**

When driving  $50\Omega$  or  $75\Omega$  back-terminated transmission lines, capacitive loading is not an issue. The MAX4102/ MAX4103 can typically drive 5pF and 20pF, respectively. Figure 3a illustrates how a capacitive load influences the amplifier's peaking without an isolation resistor (Rs). Figure 3b shows how an isolation resistor decreases the amplifier's peaking. By using a small isolation resistor between the amplifier output and the load, large capacitance values may be driven without oscillation (Figure 4a). In most cases, less than 50 $\Omega$  is sufficient. Use Figure 4b to determine the value needed in your application. Determine the worst-case maximum capacitive load you may encounter and select the appropriate resistor from the graph.

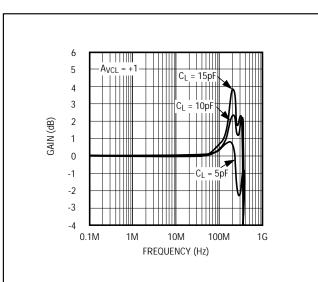


Figure 3a. MAX4102 Bandwidth vs. Capacitive Load (No Isolation Resistor ( $R_S$ ))

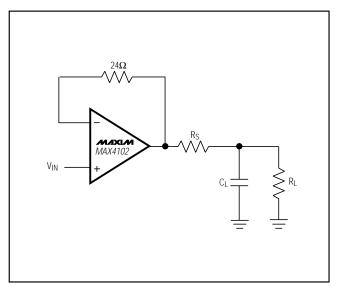


Figure 4a. Using an Isolation Resistor (R<sub>S</sub>) for Large Capacitive Loads (MAX4102)

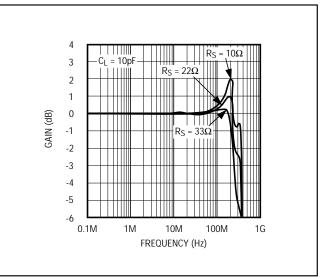


Figure 3b. MAX4102 Bandwidth vs. 10pF Capacitive Load and Isolation Resistor

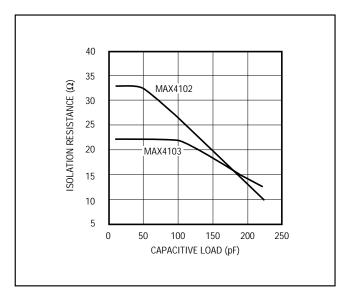
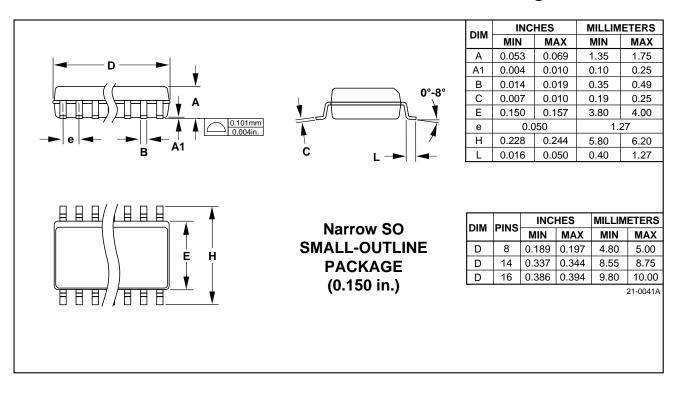


Figure 4b. Isolation vs. Capacitive Load



### \_Package Information



Chip Information

TRANSISTOR COUNT: 51 SUBSTRATE CONNECTED TO: VEE

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